



Attorney Docket SEL 162-270

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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#11
Bull

In Re Application of)
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Shunpei Yamazaki et al.)
)
Serial No.: 09/507,825)
)
Filed: February 22, 2000)
)
For: Time And Voltage Gradation)
Driven Display Device)
)
Art Unit: 2673)
)
Examiner: D. Lewis)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:
the Assistant Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450 on

May 2, 2003
(Date of Deposit)

Shannon Wallace
Name of applicant, assignee or Registered Rep.

Shannon Wallace 5/2/03
Signature Date

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Technology Center 2300

RESPONSE (B) AFTER FINAL

Sir:

Applicants have the following response to the Final Rejection of December 4, 2002, a two month extension of time being separately submitted.

Claims Rejections - 35 USC §§102, 103

The Examiner rejects Claims 1-4, 11-14, 21-24, 31-34, 41-44, 51-54, 61-64 and 71-74 under 35 U.S.C. §102(e), as being anticipated by Kubota et al. and Claims 5-10, 15-20, 25-30, 35-40, 45-50, 55-60, 65-70 and 75-80 under 35 U.S.C. §103(a) as being unpatentable over Kubota et al. in view of Takano et al. and Hasegawa et al. These rejections are respectfully traversed.

The claims of the present application, such as for example independent Claim 1, are directed to a display device in which gradation voltage and time gradation are both used. It is respectfully submitted that the cited references do not disclose or suggest such a display device.

In the Office Action, the Examiner alleges that Kubota discloses the claimed display device and in particular that Kubota “teaches of n bit input data, wherein gradation voltage and time voltage are both used” and cites to col. 22, lns. 27-67, col. 23, lns. 15-67 and col. 25, lns. 29-51 of Kubota in support thereof. The Examiner also cites to Fig. 1 of Kubota in support of his rejection. Applicants respectfully disagree with this allegation.

Kubota teaches that a n-bit digital signal is sampled by the sampling circuit 12, and thereafter divided into m-bit and k-bit, over a period 2^k , wherein one of the gradation voltage is outputted. See col. 23, lns. 18-45. Further, Kubota states “...a desired gradation voltage V is outputted to the source line SL during one period of the 2^k periods.” Col. 23, lns. 43-45

Applicants, however, respectfully submit that Kubota does not teach or suggest time gradation, as required in the claims of the present application. More specifically, time gradation is not the one gradation outputted during one period of the 2^k period.

In particular, the time gradation taught in the present application plays a part in increasing the number of gradation voltage levels for the display device. See e.g. p. 13, lns. 17-20 of the present application (“The D/A converter circuit of this embodiment can output four patterns of gradation voltage levels, namely VL, VL + Δ , VL + 2 Δ , and VL + 3 Δ ...Then combining them with the time gradation display, the present invention may increase the number of gradation display levels for the display device.”). This is different than what is taught in Kubota.

Hence, Applicants respectfully submit that Kubota teaches only gradation voltage and not time gradation, as required by the claims of the present application.

Accordingly, it is respectfully submitted that the cited references fail to disclose or suggest the claimed invention. Therefore, the claims are patentable over the references and should be allowed.

Conclusion

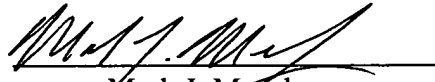
It is respectfully submitted that the present application is in a condition for allowance.

If any fee is due for this response, please charge our Deposit Account No. 50-1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: *May 2, 2007*


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